



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,294	04/22/2004	Yong-Uk Lee	YOM-0266	7218

23413 7590 05/14/2008
CANTOR COLBURN, LLP
20 Church Street
22nd Floor
Hartford, CT 06103

EXAMINER

ABDULSELAM, ABBAS I

ART UNIT	PAPER NUMBER
----------	--------------

2629

MAIL DATE	DELIVERY MODE
-----------	---------------

05/14/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/829,294	Applicant(s) LEE ET AL.	
	Examiner ABBAS I. ABDULSELAM	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 February 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7,9-12,14 and 16-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7,9-12,14 and 16-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to a communication filed on 02/20/08. Claims 1-7, 9-12, 14 and 16-22 are pending. Claims 8, 13, 15 and 23 are canceled.

Response to Arguments

2. Applicant argues (on pages 8-10 of "Remarks") about the rejections made based on 35 U.S.C. 112 first and second paragraphs. In response the examiner withdraws the rejections based on 112 first and second paragraphs. However, Applicant's other arguments filed on 02/20/08 have been fully considered but they are not persuasive.

Regarding claim 14, applicant argues neither Hasegawa (USPN 7173602) nor Drzaic (USPN 7030412) teaches or suggests "a gate line extends in a first direction, a data line which extends in a second direction substantially perpendicular to the first direction; a first pixel electrode disposed in a first region restricted by the gate line and the data line, and a second pixel electrode disposed in a second region restricted by the gate and the data line and disposed adjacent to the first region such that one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode".

The examiner disagrees with the applicant's argument. Hasegawa teaches a gate line (201) and data lines (203) as shown in Fig. 8 also see col. 10, lines 1-2. Clearly from Fig. 8, it is illustrated that the data line 203 and the gate line 201 extend in their respective directions and

intersect at right angle. With respect to the Drzaic reference, the Drzaic reference was replaced by Hanazawa et al. (USPN 5953088) reference in response to new claim limitations of the claim.

With respect to claim limitations, “a first pixel electrode disposed in a first region restricted by the gate line and the data line, and a second pixel electrode disposed in a second region restricted by the gate and the data line and disposed adjacent to the first region such that one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode”, these limitations are new claim limitations, which require the use of Hanazawa reference (see the rejection below). As mentioned above, the Hanazawa reference replaces the Drzaic reference to read over the new claim limitations as shown in the rejection below. Hence, applicant's arguments in this regard are moot in view of new grounds of rejection below.

Applicant describes the gate line and data line of the Drzaic reference with respect to Fig. 2 and Fig. 4A, and argues that in Drzaic, neither the gate lines nor the data lines overlap portions of both a first pixel electrode and a second pixel electrode. Applicant also argues in Drzaic, that no portion of the gate line overlaps any portions of any pixels and no portions of data lines overlaps any portion of any pixels.

The examiner disagrees with the applicant's arguments. Applicant argues the new claim limitations with respect to Drzaic reference. As mentioned above, Hanazawa reference replaces the Drzaic reference because of new claim limitations. Hence, applicant's arguments in this regard are moot in view of new grounds of rejection below.

On page 11 (the last paragraph), and on page 12 (the first and last paragraph) of the “Remarks”, applicant repeated the same arguments raised earlier, in response, the examiner maintains the same response as addressed earlier.

In addition, on page 12 of the remarks”, applicant describes the Drzaic reference with respect to fig. 9, and argues that Drzaic reference does not teach or suggest and it would not be obvious to extend Drzaic portion of a given pixel over the pixels’ respective gate line in addition to extending the pixel over a preceding gate line. The examiner disagrees with the applicant’s argument. As mentioned above, Hanazawa reference replaces the Drzaic reference because of new claim limitations. In addition, the applicant’s argument is about a rational used with respect to Drzaic reference over claim limitations which are now canceled by the applicant.

Regarding claims 1 and 20, applicant argues that the cited references Amundsen et al. (USPN 6545291) and Drzaic et al. (USPN 7030412) do not teach “a gate line, which extends in a first direction, a data line which extends in a second direction substantially perpendicular to the first direction; a first pixel electrode disposed in a first region restricted by the gate line and the data line, and a second pixel electrode disposed in a second region restricted by the gate and the data line and disposed adjacent to the first region such that one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode”.

The examiner disagrees with the applicant’s argument, Amundsen teaches a select line 310 and a data line 330 as shown in Fig. 5A (col. 12, lines 27, col. 10, lines 53). Clearly from Fig. 5A, it is illustrated that the select line 310 and the data line 330 extend in their respective directions and intersect at right angle. With respect to the Drzaic reference, the Drzaic reference

was replaced by Hanazawa et al. (USPN 5953088) reference in response to new claim limitations of the claim.

With respect to claim limitations, “a first pixel electrode disposed in a first region restricted by the gate line and the data line, and a second pixel electrode disposed in a second region restricted by the gate and the data line and disposed adjacent to the first region such that one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode”, these limitations are new claim limitations, which require the use of Hanazawa reference (see the rejection below). As mentioned above, the Hanazawa reference replaces the Drzaic reference to read over the new claim limitations as shown in the rejection below. Hence, applicant's arguments in this regard are moot in view of new grounds of rejection below.

Applicant further argues that in Drzaic, neither the gate lines not the data lines overlap portions of both a first pixel electrode and a second pixel electrode. Applicant also argues in Drzaic, that no portion of the gate line overlaps any portions of any pixels and no portions of data lines overlaps any portion of any pixels.

The examiner disagrees with the applicant's arguments. Applicant argues the new claim limitations with respect to Drzaic reference. As mentioned above, Hanazawa reference replaces the Drzaic reference because of new claim limitations. Hence, applicant's arguments in this regard are moot in view of new grounds of rejection below.

On page 14 (the third paragraph and the fourth paragraph) of the “Remarks”, applicant repeated the same arguments raised earlier, in response, the examiner maintains the same response as addressed earlier.

Regarding claim 7, applicant argues that the cited references Drzaic (USPN 6518949) and Drzaic et al. (USPN 703412) do not teach “a gate line extends in a first direction, a data line which extends in a second direction substantially perpendicular to the first direction; a first pixel electrode disposed in a first region restricted by the gate line and the data line, and a second pixel electrode disposed in a second region restricted by the gate and the data line and disposed adjacent to the first region such that one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode”.

The examiner disagrees with the applicant’s arguments. Drzaic (USPN 6518949) teaches a row electrode 106 and a column electrode 104 as shown in Fig. 7. Clearly from Fig. 7, it is illustrated that the row electrode 106 and the column electrode 104 extend in their respective directions and intersect at right angle (col. 8, lines 55-61), note that the same thing holds true with respect to Fig. 1c in which a row electrodes 17' and a column electrodes 15' are illustrated, and also note that the semicircular arc at the intersection of the row electrode 106 and the column electrode 104 in Fig. 7 is only for illustration purpose. With respect to the Drzaic et al. (USPN 703412) reference, the Drzaic et al. (USPN 703412) reference was replaced by Hanazawa et al. (USPN 5953088) reference in response to new claim limitations of the claim.

With respect to claim limitations, “a first pixel electrode disposed in a first region restricted by the gate line and the data line, and a second pixel electrode disposed in a second

region restricted by the gate and the data line and disposed adjacent to the first region such that one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode”, these limitations are new claim limitations, which require the use of Hanazawa reference (see the rejection below), As mentioned above, the Hanazawa reference replaces the Drzaic et al. (USPN 703412) reference to read over the new claim limitations as shown in the rejection below. Hence, applicant's arguments in this regard are moot in view of new grounds of rejection below.

Applicant further argues in Drzaic et al. (USPN 703412) reference, no portion of the gate line overlaps any portions of any pixels, and no portions of data lines overlaps any portion of any pixels.

The examiner disagrees with the applicant's arguments. Applicant argues the new claim limitations with respect to Drzaic et al. (USPN 703412) reference. As mentioned above, Hanazawa reference replaces the Drzaic et al. (USPN 703412) reference because of new claim limitations. Hence, applicant's arguments in this regard are moot in view of new grounds of rejection below.

Applicant argues that dependent claims 3 and 6 depending on claim 1, and dependent claim 22 depending on claim 20 are allowable by the virtue of their amended independent claims.

The examiner disagrees with the applicant's argument. As mentioned above, applicant's argument in this regard is moot in view of new grounds of rejection below.

Applicant argues that dependent claims 9 and 12 depending on claim 7 are allowable by the virtue of the amended independent claim 7.

The examiner disagrees with the applicant's argument. As mentioned above, applicant's argument in this regard is moot in view of new grounds of rejection below.

Applicant argues that dependent claim 10 depending on claim 7 is allowable by the virtue of the amended independent claim 7.

The examiner disagrees with the applicant's argument. As mentioned above, applicant's argument in this regard is moot in view of new grounds of rejection below.

Applicant argues that dependent claims 16 and 19 depending on claim 14 are allowable by the virtue of the amended independent claim 14.

The examiner disagrees with the applicant's argument. As mentioned above, applicant's argument in this regard is moot in view of new grounds of rejection below.

Applicant argues that dependent claims 17 and 18 depending on claim 14 are allowable by the virtue of the amended independent claim 14.

The examiner disagrees with the applicant's argument. As mentioned above, applicant's argument in this regard is moot in view of new grounds of rejection below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2629

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2 and 20-21 are rejected under 35 U.S.C. 103(a) as unpatentable over Amundson et al. (USPN 6545291) in view of Hanazawa et al. (USPN 5953088).

Regarding claim 1, Amundson et al. (hereinafter = "Amundson") teaches an electrophoretic display (*col. 4, lines 54-55*), comprising: a gate line which extends in a first direction (*col. 12, line 27, Fig. 5A (310), select line (310)*); a data line which extends in a second direction in a second direction substantially perpendicular to the first direction, (*col. 10, line 53, Fig. 5A (330), data line (330), as shown in Fig. 5A, the select line (310) is perpendicular to the data line (330)*); a first pixel electrode disposed in a first region restricted by the data line (*col. 2, lines 54-58, the pixel electrode and the data line electrode are interdigitated such that the data line electrode comprises a data line of the display, and Fig. 5a (330, 320), Fig. 5A clearly shows that a data line (330) and a pixel electrode (320) are configured to be one on top of the other or overlaps*),

Amundson does not teach a first pixel electrode disposed in a first region restricted by the gate line and the data line, and a second pixel electrode disposed in a second region restricted by the gate and the data line and disposed adjacent to the first region such that one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode.

Hanazawa on the other hand illustrates as shown in Fig. 3, adjacent two pixel electrodes (51, 54)(PE), a signal line 50a, and a scanning line Y

(62') such that parts of the pixel electrodes (51, 54) are inside the signal line (50a) and the scanning line Y (62'). Hence, as can be seen in Fig. 3, portions the pixel electrodes (51, 54) overlap both the signal line (50) and the scanning line Y (62'), and also note that from Fig. 3, pixel electrodes (51, 54) have their respective regions with respect to the signal line 50a and the scanning line Y(62) are (col. 4, lines 11-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Amundson's pixel electrode (320) shown in Fig. 5B with Hanazawa's use pixel electrodes (51, 54) as configured in Fig. 3, because the use of two pixel electrodes helps suppress an increase in the capacitive load of a signal line without impairing an electrostatic shielding property, and obtain a high aperture ratio as taught by Hanazawa (col. 2, lines 19-32).

Regarding claim 20, Amundson teaches an electrophoretic display (*col. 4, lines 54-55*), comprising; a gate line which extends in a first direction (*col. 12, line 27, Fig. 5 (310), select line (310)*); a data line which extends in a second direction substantially perpendicular to the first direction (*col. 10, line 53, Fig. 5A (330), data line (330), as shown in Fig. 5A, the select line (310) is perpendicular to the data line (330)*); a first pixel electrode disposed in a first region restricted by data line (*col. 2, lines 54-58, the pixel electrode and the data line electrode are interdigitated such*

that the data line electrode comprises a data line of the display, and Fig. 5a (330, 320), Fig. 5A clearly shows that a data line (330) and a pixel electrode (320) are configured to be one on top of the other or overlaps); a common electrode (col. 7, lines 43-45, bounding electrodes, col. 8, lines 19-24, multiple pair of electrodes (30, 40) per capsule (20), it is obvious in the electrophoretic display that one of the bounding electrode is a common electrode); and a plurality of micro-capsules (col. 8, lines 39-43, Fig. 1 (20), multiple capsules 20 may be positioned, col. 7, lines 35-38, individual electrophoretic phases may be referred as capsules or microcapsules), wherein each microcapsule of the microcapsules of the plurality of microcapsules comprises electric ink containing a plurality of color pigment particles, (col. 6, lines 12-19, particles may be encapsulated in the capsules, and include dyed pigments and are dispersed in a suspending fluid, and col. 7, lines 54-55, Fig. 1A (20, 25, 50), a capsule (20) contains at least one particle (50) dispersed in a suspending fluid (25)), wherein a color of the plurality of color pigment particles is at least one of red, green, blue, cyan, yellow, magenta black and white (col.8, lines 5-6, particles may be colored any one of a number of colors, and col. 9, lines 31-32, blue particles).

Amundson does not teach a first pixel electrode disposed in a first region restricted by the gate line and the data line, and a second pixel electrode disposed in a second region restricted by the gate and the data line and disposed adjacent to the first region such that one of the gate line

and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode.

Hanazawa on the other hand illustrates as shown in Fig. 3, adjacent two pixel electrodes (51, 54)(PE), a signal line 50a, and a scanning line Y (62') such that parts of the pixel electrodes (51, 54) are inside the signal line (50a) and the scanning line Y (62'). Hence, as can be seen in Fig. 3, portions the pixel electrodes (51, 54) overlap both the signal line (50) and the scanning line Y (62'), and also note that from Fig. 3, pixel electrodes (51, 54) have their respective regions with respect to the signal line 50a and the scanning line Y(62) are (col. 4, lines 11-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Amundson's pixel electrode (320) shown in Fig. 5B with Hanazawa's use pixel electrodes (51, 54) as configured in Fig. 3, because the use of two pixel electrodes helps suppress an increase in the capacitive load of a signal line without impairing an electrostatic shielding property, and obtain a high aperture ratio as taught by Hanazawa (col. 2, lines 19-32).

Regarding claims 2 and 21, Hanazawa teaches the portion of the first pixel electrode and the portion of the second pixel electrode overlap a portion of a width of the data line extending in the second direction between adjacent gate lines (*Fig. 3 (51, 54), col. 4, lines 11-27, see fig. 3 in which portions of pixel electrodes (51, 54) overlap with a*

portion of signal line 50a, also Fig. 3 shows the signal line 50a extends throughout the scanning line (62', 62)Y).

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Hanazawa et al. (USPN 5953088).

Regarding claim 14, Hasegawa et al. (hereinafter = "Hasegawa") teaches an electrophoretic display comprising (*col. 6, lines 55-56, an electronic ink display*); substrate (*col. 9, line 14, Fig. 7 (501) an insulating substrate (501)*); and a thin film transistor formed on a surface of the substrate (*col. 9, line 9, a TFT*) this thin film transistor comprising a source electrode and a drain electrode formed on the substrate (*col. 9, lines 11-14, Fig. 7 (403, 501), an electrode layer (403), which is a source-drain electrode formed on an insulating substrate (501)*); a semiconductor layer formed on the source and the drain electrode (*col. 9, lines 9-14, Fig. 7 (401, 403), the electrode layer (403) and polycrystalline silicon layer (401), col. 9, lines 11-14, Fig. 7 (403, 501), an electrode layer (403), which is a source-drain electrode formed on an insulating substrate (501)*); an insulation layer formed on the semiconductor layer (*col. 9, lines 9-10, Fig. 7 (502, 401) a gate insulating film (502) and the polycrystalline silicon layer (401));* and a gate electrode formed on the insulation layer (*col. 9, lines 10, Fig. 7 (502, 503), the gate insulating film (502) and gate electrode (503)*), a gate line which extends in a first direction(*col. 10,*

lines 1-2, Fig. 8 (201) a gate line); a data line which extends in a second direction substantially perpendicular to the first direction (col. 10, lines 1-2, Fig. 8 (203), data line (203));

Hasegawa does not teach a first pixel electrode disposed in a first region restricted by the gate line and the data line, and a second pixel electrode disposed in a second region restricted by the gate and the data line and disposed adjacent to the first region such that one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode.

Hanazawa on the other hand illustrates as shown in Fig. 3, adjacent two pixel electrodes (51, 54)(PE), a signal line 50a, and a scanning line Y (62') such that parts of the pixel electrodes (51, 54) are inside the signal line (50a) and the scanning line Y (62'). Hence, as can be seen in Fig. 3, portions the pixel electrodes (51, 54) overlap both the signal line (50) and the scanning line Y (62'), and also note that from Fig. 3, pixel electrodes (51, 54) have their respective regions with respect to the signal line 50a and the scanning line Y(62) are (col. 4, lines 11-27).

Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's electrophoretic display shown in Fig. 8 with Hanazawa's pixel electrodes (51, 54) as configured in Fig. 3, because the use of two pixel electrodes helps suppress an increase in the capacitive load of a signal line without impairing an

electrostatic shielding property, and obtain a high aperture ratio as taught by Hanazawa (col. 2, lines 19-32).

5. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drzaic (USPN 6518949) in view of Hanazawa et al. (USPN 5953088).

Regarding claim 7, Drzaic (USPN 6518949) teaches an electrophoretic display (*col. 1, line 59-61, col. 1, line 67 and col. 2, lines 1-2 and Fig. (8)*) comprising; **a** substrate (*Fig. 8(92'), substrate 92'*); a gate line which extends in a first direction (*Fig. 7 (106), row electrode 106*); **a** data line which extends in a second direction substantially perpendicular to the first direction (*Fig. 7 (104), a column electrode 104, as shown in Fig. 7, the column electrode 104 is perpendicular to the row electrode 106*); a first thin film transistor comprising a first channel (*Fig. 8 (90'), transistor (90')*); a first gate electrode (*col. 10, lines 9, Fig. 8 (96'), gate electrode (96')*), a first source electrode (*col. 10, lines 7, Fig. 8(98'), source electrode (98')*); a first drain electrode and a first semiconductor layer (*col. 10, line 8, col. 10, lines 4, Fig. 8(99', 97'), a drain electrode 99' and a semiconductor layer 97'*); a first opaque layer (*col. 10, line 6, Fig. 8(110) a barrier layer (110), and col. 9, lines 50-51, a barrier layer is opaque*) formed on the first semiconductor layer and disposed over the channel of the first thin film transistor (*col. 10, lines 3-4, the barrier layer (110) is positioned over at least a semiconductor layer (97'), and Fig. 8 (96', 110, 97'), Fig. 8 shows the semiconductor layer 97' is between the gate*

electrode, 96' and the barrier layer (110)); a second thin film transistor disposed adjacent to the first thin film transistor (Fig. 9 (90'), see Fig. 9 in which the two identical transistor 90' are located adjacent to each other) and comprising a second channel (Fig. 8 (90'), transistor (90')); a second gate electrode (col. 10, lines 9, Fig. 8 (96'), gate electrode (96')); a second source electrode (col. 10, lines 7, Fig. 8 (98'), source electrode (98')); and a second drain electrode and a second semiconductor layer (col. 10, line 8, col. 10, lines 4, Fig. 8 (99', 97'), a drain electrode 99' and a semiconductor layer 97'); a second opaque layer (col. 10, line 6, Fig. 8 (110) a barrier layer (110), and col. 9, lines 50-51, a barrier layer is opaque) formed on the second semiconductor layer and disposed over the channel of the second thin film transistor (col. 10, lines 3-4, the barrier layer (110) is positioned over at least a semiconductor layer (97'), and Fig. 8 (96', 110, 97'), Fig. 8 shows the semiconductor layer 97' is between the gate electrode, 96' and the barrier layer (110)) a first pixel electrode disposed over the first thin film transistor; and a second pixel electrode disposed over the second thin film transistor (col. 2, lines 17-20, use of a plurality of pixel electrodes, col. 9, line 67 and col. 10, line 1, as shown in Fig. 8 (90', 92', 124), each transistor 90' is positioned adjacent to a pixel electrode 124 on a substrate 92', col. 4, lines 24-25, Fig. 1 (18, 20), it is also known that the transistor (20) are located underneath a pixel electrode 18),

Hasegawa does not teach a first pixel electrode and a second pixel electrode such that one of the gate line and the data line is interposed between the first pixel electrode and the second pixel electrode and overlaps a portion of the first pixel electrode and a portion of the second pixel electrode.

Hanazawa on the other hand illustrates as shown in Fig. 3, adjacent two pixel electrodes (51, 54)(PE), a signal line 50a, and a scanning line Y (62') such that parts of the pixel electrodes (51, 54) are inside the signal line (50a) and the scanning line Y (62'). Hence, as can be seen in Fig. 3, portions the pixel electrodes (51, 54) overlap both the signal line (50) and the scanning line Y (62'), and also note that from Fig. 3, pixel electrodes (51, 54) have their respective regions with respect to the signal line 50a and the scanning line Y(62) are (col. 4, lines 11-27).

Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to combine Drzaic's pixel electrode (124) shown in Fig. 8 with Hanazawa's pixel electrodes (51, 54) as configured in Fig. 3, because the use of two pixel electrodes helps suppress an increase in a capacitive load of a signal line without impairing an electrostatic shielding property, and obtain a high aperture ratio as taught by Hanazawa (col. 2, lines 19-32).

Regarding claim 11, Drzaic's (USPN 6518949) teaches wherein the first pixel electrode is made of opaque material (col. 2, lines 38-41, a substrate that can be opaque,

and col. 8, lines 15-17, a substrate that can be patterned to serve as the pixel electrode), and wherein the first pixel electrode and the second overlap the channel of the thin film transistor (col. 4, lines 23-25, Fig. 1a (20) the transistors 20 are located underneath the pixel electrodes (18)).

6. Claim 5 is rejected under 35 U.S.C. 103(a)) as unpatentable over Amundson et al. (USPN 6545291) in view of Hanazawa et al. (USPN 5953088) and further in view of Drzaic et al. (USPN 7030412).

Regarding claim 5, Amundson (as modified by Hanazawa) teaches a thin film transistor comprising a channel (*col. 11, lines 36-37, Fig. 4B, a TFT with a channel*); a source electrode (*col. 11, lines 6-7, Fig. 5A(120), a source electrode (120)*); a drain electrode (*col. 11, lines 6-7, Fig. 5A (130), a drain electrode (130)*); and wherein the first pixel electrode and the second pixel electrode overlaps the channel of the thin film transistor (*col. 11, lines 45-47, a TFT channel is substantially under the pixel electrode*),

While Amundson (as modified by Hanazawa) teaches electrodes (30, 40) that could be fabricated from opaque materials (col. 8, lines 55-56),

Amundson in view of Hanazawa does not teach the first pixel electrode and the second pixel electrode are made of opaque material.

Drzaic et al. (USPN 7030412) on the other hand teaches a pixel electrode (104) as shown in Fig. 10 that can be transparent or opaque (col. 10, lines 61-62 and Fig. 10 (104)).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Amundson's pixel electrode (320) (as modified by Hanazawa) shown in Fig. 5A with Drzaic's opaque characteristics of the pixel electrode (104), because the use of an opaque pixel electrode helps function an electronic display 100 by being bonded to a display medium as taught by Drzaic (col. 8, lines 52-56).

7. Claims 3, 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amundson et al. (USPN 6545291) in view of Hanazawa et al. (USPN 5953088) and further in view of Yamamoto et al. (USPN 6563260).

Regarding claims 3, 6 and 22, while Amundson (as modified by Hanazawa) teaches an insulating layer is/interposed/formed between the data line and one of the first pixel electrode and the second pixel electrode(*col. 11, lines 17-20, an insulating layer (170) separating a drain electrode (130) from the pixel electrode (320), and col. 10, lines 52-53, Fig. 3 (130, 330), the drain electrode (130) of TFT is connected to a data line 330*),

Amundson (as modified by Hanazawa) does not teach the insulating layer having a dielectric constant lower than 4, with the insulating layer being made of a-Si:C:O or a-Si:O:F.

Yamamoto et al. (USPN 6563260) on the other hand teach a dielectric constant of an insulating layer, which could be formed of silicone oxide containing fluorine, being equal or less than 4 as plotted in Fig. 3 (col. 13, lines 59-64 and col. 13, lines 48-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Amundson's (as modified by Hanazawa) insulating layer (170) of an electrophoretic display shown in Fig. 5B with Yamamoto's insulating layer (made of silicone oxide containing fluorine) having less than 4 dielectric constant, because the use of such insulation layer with a dielectric constant of less than 4 helps manufacture a field emission display whose emitter layer is formed by electrophoresis as taught by Yamamoto (col. 9, lines 9-10, col. 9, lines 16-18 and col. 13, lines 59-60).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Amundson et al. (USPN 6545291) in view of Hanazawa et al. (USPN 5953088) and further view of Izumi et al. (USPN 7148867).

Regarding claim 4, *while Amundson (as modified by Hanazawa) teaches various materials may be used to create electrophoretic displays, and cites as exemplary particles including titania, which may be coated in one or two layers in a metal oxide (col. 6, lines 52-54 and col. 6, lines 61-63),*

Amundson (as modified by Hanazawa) does not teach “the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti”.

Izumi et al. (USPN 7148867) on the other hand teaches source lines (25) may be formed by patterning a metal film of Ta, or Mo as shown in Fig. 1B (col. 8, lines 10-13).

Note that even though Amundson teaches electrophoretic display and Izumi teaches liquid crystal display, the functionality of Amundson’s data line (330) and Izumi’s source line (25) is the same for both types of displays.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Amundson’s data line (330) of an electrophoretic display shown in Fig. 5A (as modified by Hanazawa) with Izumi’s Tantalum (Ta)-patterned metal film, because the use of Tantalum (Ta)-patterned metal film with respect to source line (25) helps constitute an addressing substrate (100B) of display device (100) as taught by Izumi (col. 7, lines 11-13, col. 7, lines 60-61 and col. 8, lines 10-13).

9 Claims 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable Drzaic (USPN 6518949) in view of Hanazawa et al. (USPN 5953088) and further in view of Yamamoto et al. (USPN 6563260).

 Regarding claims 9 and 12, while Drzaic (as modified by Hanazawa) teaches an insulating layer formed between the data line and one of the first pixel electrode and the second pixel electrode (*col. 4, lines 61-65, Fig. 1 C (18', 21, 15'), a pixel electrode (18') and a column electrode 15' and insulator (21) are configured*),

 Drzaic does not teach the insulating layer having a dielectric constant smaller than 4 with the insulating layer being made of a-Si:C:O or a-Si:O:F.

Yamamoto et al. (USPN 6563260) on the other hand teach a dielectric constant of an insulating layer, which could be formed of silicone oxide containing fluorine, being equal or less than 4 as plotted in Fig. 3 (col. 13, lines 59-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Drzaic's (as modified by Hanazawa) insulator (21) of an electronic display shown in Fig. 1c with Yamamoto's insulating layer (made of silicone xide containing fluorine) having less than 4 dielectric constant, because the use of such insulation layer with a dielectric constant of less than 4 helps manufacture a field

emission display whose emitter layer is formed by electrophoresis as taught by Yamamoto (col. 9, lines 9-10, col. 9, lines 17-19 and col. 13, lines 59-60).

10 Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Drzaic (USPN 6518949) in view of Hanazawa et al. (USPN 5953088)) and further in view of Izumi et al. (USPN 7148867).

Regarding claim 10, while Drzaic (as modified by Hanazawa) *teaches formation of column electrodes through conductive coatings, which may be Indium, Tin Oxide (ITO) or some other suitable conductive material (col. 11, lines 10-13, col. 11, lines 19-20),*

Drzaic (as modified by Hanazawa) does not specifically teach “the data line is made of metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti”.

Izumi et al. (USPN 7148867) on the other hand teaches source lines (25) that may be formed by patterning a metal film of Ta, or Mo as shown in Fig. 1B (col. 8, lines 10-13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Drzaic's (as modified by Hanazawa) column electrode (104) of an electronic display shown in Fig. 7

with Izumi's use of Tantalum (Ta)-patterned metal film for source lines, because the use of Tantalum (Ta)-patterned metal film with respect to source line (25) helps constitute an addressing substrate (100B) of a display device (100) as taught by Izumi.

11 Claim 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Hanazawa et al. (USPN 5953088). and further in view of Yamamoto et al. (USPN 6563260).

Regarding claims 16 and 19, While Hasegawa (as modified by Hanazawa) teaches an insulating layer is formed between the data line and one of the first pixel electrode and the second pixel electrode, (*col. 9, lines 10-11, col. 9, lines 15-16, col. 10, lines 5-6, Fig. 7 (403, 502, 504, 405), an electrode layer (403), interlayer insulating film (504) & gate insulating film (502), and pixel electrode (405)*),

Hasegawa (as modified by Hanazawa) does not teach the insulating layer has a dielectric constant smaller than 4.

Yamamoto et al. (USPN 6563260) on the other hand teach a dielectric constant of an insulating layer, which could be formed of silicone oxide containing fluorine, being equal or less than 4 as plotted in Fig. 3 (col. 13, lines 59-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's (as modified by Hanazawa) insulating films (502, 504) of an electrophoretic display shown in Fig. 7 with Yamamoto's insulating layer (made of silicone oxide containing fluorine) having less than 4 dielectric constant, because the use of such insulation layer with a dielectric constant of less than 4 helps manufacture a field emission display whose emitter layer is formed by electrophoresis as taught by Yamamoto (col. 9, lines 9-10, col. 9, lines 17-19 and col. 13, lines 59-60).

12 Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Hanazawa et al. (USPN 5953088) and further in view of Izumi et al (USPN 7148867).

Regarding claim 17, *while Hasegawa (as modified by Hanazawa) teaches electrode layers including a layer of titanium (col. 3, lines 53-55),*

Hasegawa (as modified by Hanazawa) does not specifically teach “the data line is made of a metal selected from a group consisting of Mo, Mo alloy, Cr, Ta and Ti”.

Izumi et al. (USPN 7148867) on the other hand teaches source lines (25) may be formed by patterning a metal film of Ta, or Mo as shown in Fig. 1B (col. 8, lines 10-13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's (as modified by Hanazawa) data line (203) of an electrophoretic display shown in Fig. 8 with Izumi's Tantalum (Ta)-patterned metal film, because the use of Tantalum (Ta)-patterned metal film with respect to source line (25) helps constitute an addressing substrate (100B) of display device (100) as taught by Izumi (col. 7, lines 11-13, col. 7, lines 60-61 and col. 8, lines 10-13).

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa et al. (USPN 7173602) in view of Hanazawa et al. (USPN 5953088) and further in view of Hirota (USPN 7098980).

Regarding claim 18, Hasegawa (as modified by Hanazawa) does not teach “ the inclination angle of the gate line or the data line relative to the surface of the substrate ranges between about 20 degrees to about 80 degrees”.

Hirota (USPN 7098980) on the other hand teaches as a scanning line (1), pixel electrodes 5 and a common electrode 6 are so configured as to be bent relative to the alignment direction of N-type liquid crystal. Hirota further teaches that the bent angle 10 can be selected to be an angle with the best display performance as long as the angle is within the range from

60 degrees to 120 degrees except 90 degrees (col. 5, lines 28-34, Fig. 5 (1, 5, 6)).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Hasegawa's (as modified by Hanazawa) gate lines (201) of a display shown in Fig. 8 with Hirota's bendable electrode having a range of bending angle (60-120 degrees, (90) excepted), which includes a range of 60-80 degrees, because the use of bendable electrode or line makes it possible to achieve a large screen, wide visual angle display with high yield and low cost as taught by Hirota (col. 5, lines 65-67).

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulsalam whose telephone number is 571-272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Abbas I Abdulsalam/

Primary Examiner, Art Unit 2629